SOMAIYA
VIDYAVIHAR

K J Somaiya Institute of Technology
An Autonomous Institute Permanently Affiliated to the University of Mumbai

Item No.
A.C. Date: --/--/2025

Autonomy Syllabus Scheme III (2023-24)

(As per NEP 2020 Guidelines)

for

Four Year Multidisciplinary

Bachelors of Technology (B. Tech.) Program

in

Electronics and Telecommunication Engineering with

Multiple Entry and Multiple Exit Options

Levels 4.5 - 6

(Third Year Effective from A.Y. 2025-26)

From the Principal's Desk:

To address the changing demands of the digital era, it is required to create a future-ready workforce that can navigate the complexities of an interconnected world, drive innovation, and contribute to the nation's growth. The **National Educational Policy 2020 (NEP 2020)** framed by the Government of India recommends a holistic, inclusive, and flexible approach to ensure equitable access to quality education across all levels, promote multidisciplinary research, and impart skill-based education with integration of technology. As per guidelines by the Department of Higher and Technical Education, Government of Maharashtra, the salient features of NEP 2020 aligned curriculum should include:

- Major (Core) Mandatory and Elective Courses
- Open Elective Courses
- Vocational and Skill Enhancement Courses
- Ability Enhancement Courses, Indian Knowledge System, and Value Education Courses
- Co-curricular Courses and Field Projects / Community Engagement Projects / Internship
- Multidisciplinary Minor Courses
- Option for Bachelor's Degree with Honours (based on Additional Credits)
- Option for Bachelor's Degree – Honours with Research (based on Additional Credits)
- Option for Bachelor's Degree with Double Minors (based on Additional Credits)
- Multiple Entry and Multiple Exit Options

Being an **autonomous institute** since the Academic Year 2021-22, **K. J. Somaiya Institute of Technology (KJSIT)**, has well-adapted newer approaches to reach higher levels of excellence in engineering education. Ahead of its time, the academic reforms at KJSIT have already addressed majority of these NEP 2020 aspects through its existing **Syllabus Scheme I, II, and II B** implemented under the academic autonomy. For a complete alignment with NEP 2020, the **KJSIT Autonomy Syllabus Scheme III** is introduced, to be effective from Academic Year 2023-24 across all the branches, progressively from First Year Engineering.

Specifically, the existing curriculum already comprise state-of-the-art **Major (Core) courses** in theory and practical. With an ideology that the root of innovation is 'interest', the curriculum offers wide range of Elective courses — grouped into **Major-related Electives** and **Inter-disciplinary / Open Electives**. At par with international engineering education, it follows a learner-centric approach as well as promotes MOOCs, where the students can choose to study courses concerning areas of their interests, and the same is continued in Scheme III.

Further, under the theme of "Learning by Doing", the existing curriculum includes Skill-Based Learning (SBL), Activity-Based Learning (ABL), and Technology-Based Learning (TBL) as eXposure (SAT) courses — that assure X factor in all the students of the institute. The SAT courses are practiced across the first three years of engineering, focusing on responsibilities towards society, problem-solving abilities, communication skills, ethics, leadership and teamwork, motivation for life-long learning, skills on emerging areas of technology, skills on different languages, etc. In the Syllabus Scheme III, these SAT courses are now aligned and offered as **Vocational Skill - SAT (VS - SAT) courses**, **Skill Enhancement - SAT (SE - SAT) courses**, **Ability Enhancement - SAT (AE - SAT) courses**, and **Value Education - SAT (VE - SAT) courses**.

Further, **Indian Knowledge System - SAT (IKS - SAT) course** is newly introduced in Scheme III that emphasizes on drawing insights from ancient wisdom to address modern challenges. Also, as an extension to the induction program for the First Year students, the introduced **Co-curricular - SAT (CC - SAT) course** aims to induct incumbents with the institutional practices, culture, and values, as well as encourage participation in co-curricular activities.

The component of **Project-Based Learning (PBL)** included in the Syllabus Scheme II is carried forward to Scheme III, wherein the students develop **Community Engagement / Field Projects** in Second, Third, and Last Year as Mini, Minor, and Major Projects respectively. Scheme III also retains the **Internship** component, offered with credits, to equip graduates with the industry trends, practices, and skills required at national and global level.

The duality of PBL and Internship enables student involvement in research, innovation, and entrepreneurship, which are the fulcrums of higher education.

As a new introduction in line with NEP 2020, the Syllabus Scheme III incorporates mandatory **Multidisciplinary Minor courses** in Innovation and Entrepreneurship, Biotechnology, IoT and Cloud Computing, Geographical Information System, Very Large Scale Integration (VLSI) and Artificial Intelligence. These courses promote interdisciplinary thinking and broaden the career prospects, enabling students to develop solutions to real-world problems by combining expertise from multiple domains.

Aligned with NEP 2020, the Scheme III retains the initiative taken through Scheme II / II B of offering **Honours courses** for students who are desirous of pursuing focused interest in 06 emerging areas of technology recognized by AICTE: Internet of Things, Artificial Intelligence & Machine Learning, Cyber Security, Virtual and Augmented Reality, Data Science, and Blockchain. These Honours courses correspond to high-end industry standards and offer multi-fold opportunities of specialization.

As per NEP 2020, the above curricular aspects of Four Years UG Engineering Programme shall be offered with **Multiple Entry and Multiple Exit options**, leading to the conferment of:

- **One Year UG Certificate in Technology:** Awarded after completing First Year of Engineering and acquiring additional 08 credits immediately after First Year.
- **Two Years UG Diploma in Technology:** Awarded after completing Second Year of Engineering and acquiring additional 08 credits immediately after Second Year.
- **Three Years Bachelor's Degree in Vocation (B.Voc.):** Awarded after completing Third Year of Engineering and acquiring additional 08 credits immediately after Third Year.
- **Four Years Bachelor's Degree in Technology (B.Tech.) with Multidisciplinary Minor:** Awarded after completing Fourth Year of Engineering.
- **Four Years Bachelor's Degree in Technology (B.Tech.) Honors with Multidisciplinary Minor:** Awarded after completing Fourth Year of Engineering and acquiring additional 18 credits through Honours courses in respective major discipline over Third & Fourth Year of Engineering.
- **Four Years Bachelor's Degree in Technology (B.Tech.) Honors with Research and Multidisciplinary Minor:** Awarded after completing Fourth Year of Engineering and acquiring additional 18 credits through a research project in respective major discipline during Fourth Year of Engineering.
- **Four Years Bachelor's Degree in Technology (B.Tech.) with Double Minors (Multidisciplinary & Specialization):** Awarded after completing Fourth Year of Engineering and acquiring additional 18 credits through additional courses in another Engg. / Tech. discipline during Second to Fourth Year of Engineering.

Through the implementation of Autonomy Syllabus Scheme III (as per NEP 2020 Guidelines), strategic planning, and joint efforts of all stakeholders, KJSIT is endeavouring to enhance the quality of engineering education and set a benchmark for all the autonomous institutes nationwide.

Dr. Vivek Sunnapwar
Principal and Chairman - Academic Council

Preface by Chairperson – Board of Studies (BoS):

In today's world, lot of technological developments are taking place in the field of Electronics & Telecommunication Engineering in order to meet the current requirements. Hence, there is always a requirement for continuous enrichment of course content in the field of education on regular basis to maintain a good quality of education by the regular revision of curriculum. This will help our students with the upgraded knowledge, help in achieving better employability, opportunities to work with start -ups, chances for good internships at premier organizations/industries and other avenues of higher studies.

The revised curriculum of Scheme-III (Electronics and Telecommunication Engineering) under the autonomy has focussed on all these above mentioned factors and aims to provide strong foundation along with required analytical concepts in the field of electronics & telecommunication. The curriculum is designed keeping in mind the guidelines of NEP-2020. Some of the salient features of the syllabus are as mentioned below.

1. The curriculum is designed with a total of number of 174 credits along with the inclusion of Skill, and Technology and Project based learning.

2. The skill based courses are introduced in the second and third year in which students are exposed to hard/ soft skills. Students are also introduced with the community engagement projects in the second year in current technologies.

3. Third year students are introduced with technology based learning along with skill based courses. The community engagement projects are introduced to the third year students in the specialized core fields

4. Students are introduced to National/Foreign Languages in the second year to make them proficient at job locations as per the requirement.

5. The curriculum is designed to incorporate the electives in (department and institute level) covering the thrust areas that will provide more focussed approach for the students in problem solving and also to be at par with the current industry requirements.

6. The contents of the curriculum is designed taking into consideration the IT domain developments into account and at the same time keeping the focus on core specialization of the program intact

7. The internships are made mandatory and credit based for all the students in semester VIII. The students are provided with the flexibility to carry out internship for entire semester. That helps them to acquaint with the industry work culture

As Chairman BOS, I take this opportunity to thank all the internal and external BOS members, subject experts, industry representatives, alumni, and various other stakeholders for their sincere efforts and valuable inputs in the preparation of course contents, in reviewing the contents and critically analysing the contents.

Dr. Jayashree V. Khanapuri
Head and Chairperson,
Electronics and Telecommunication Engineering Department, KJSIT

Board of Studies (BoS) in Electronics and Telecommunication Engineering – K. J. Somaiya Institute of Technology (KJSIT):

1. **Dr. Jayashree Khanapuri**
   Professor and Head – Department of Electronics and Telecommunication Engineering,
   Chairperson – BoS in Electronics and Telecommunication Engineering, KJSIT
2. **Dr. Namrata Ansari**
   Professor – Department of Electronics and Telecommunication Engineering and Dean – Academics, KJSIT
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   Assistant Professor – Department of Electronics and Telecommunication Engineering, KJSIT
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7. **Dr. Kiran Rathod**
   Assistant Professor – Department of Electronics and Telecommunication Engineering, KJSIT
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12. **Ms. Rupali Satpute**
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19. **Dr. Priya Hankare**
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20. **Ms. Swati Shinde**
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21. **Mr. Sagar Mhatre**
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22. **Dr. Deepak Bhoir**
    Professor and Dean Academics, Fr. Conceicao Rodrigues College of Engineering, Bandra, Mumbai
23. **Dr. Virendra Shete**
    Professor, MIT – School of Engineering, Pune
24. **Dr. Vivek Agarwal**
    Professor, Department of Electrical Engineering, IIT Bombay
25. **Mr. Alister D'silva**
    Director, Absolute Motion Pvt. Ltd., Mumbai

Nomenclature and Alignment of Verticals and Components

Verticals as per NEP 2020 Guidelines	Components Aligning with KJSIT Autonomy Syllabus Scheme I / II / II B	Nomenclature for KJSIT Autonomy Syllabus Scheme III Aligned with NEP 2020 Guidelines
Basic and Engineering Science Courses	Basic Science (BS) Course	Basic Science (BS) Courses
	Engineering Science (ES) Course	Engineering Science (ES) Courses
Major Courses	Professional Core (PC) Courses	Major / Professional Core (PC) Courses
	Professional Elective - Department-level (PE-DLC) Courses	Major / Professional Elective - Department-level (PE-DLC) Courses
Generic / Open Elective Courses	Open Elective - Institute-level (OE-ILC) Courses	Open Elective - Institute-level (OE-ILC) Courses
Multidisciplinary Minor Courses	-	Multidisciplinary Minor (MM) Courses
Vocational Skill Courses	Workshop I; Workshop II; SAT Courses – TBL	Vocational Skill - SAT (VS-SAT) Courses
Skill Enhancement Courses	SAT Courses – SBL (Program Specific)	Skill Enhancement - SAT (SE-SAT) Courses
Ability Enhancement Courses	Professional Communication Skills; SAT Course – SBL (Foreign and/or Indian Modern Languages)	Ability Enhancement - SAT (AE - SAT) Courses
Indian Knowledge System Courses	-	Indian Knowledge System - SAT (IKS - SAT) Courses
Value Education Courses	SAT Course – ABL (National, Global, Societal and Environmental Aspects); Business Communication & Ethics	Value Education - SAT (VE - SAT) Courses
Field Projects / Community Engagement Projects	PBL – Mini, Minor, Major	Community Engagement – Project-Based Learning (PBL)
Internship / Apprenticeship	Internship	Internship (INT)
Co-curricular Courses	Student Induction Program	Co-curricular - SAT (CC - SAT) Courses

Other Abbreviations:

- SAT – Skill/Activity/Technology-Based Learning (Exposure Courses)
- TH – Theory
- P – Practical
- TUT – Tutorial
- T1 – Test 1
- T2 – Test 2
- CA – Continuous Assessment Test (T = T1 + T2)
- ESE – End Semester Exam
- TW – Term Work
- O – Oral Exam
- P – Practical Exam
- P&O – Practical & Oral Exam

Programs Offered with Multiple Entry Multiple Exit Options

Level 4.5: UG Certificate in Technology

Major Discipline:	Electronics and Telecommunication Engineering
Years of Study:	01 Year
Semesters:	1 and 2
Credits:	42
Additional Requirements:	08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major during Summer Vacation after 1st Year

Level 5: UG Diploma in Technology

Major Discipline:	Electronics and Telecommunication Engineering
Years of Study:	02 Years
Semesters:	1, 2, 3, 4
Credits:	85
Additional Requirements:	08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major during Summer Vacation after 2nd Year

Level 5.5: Bachelor's Degree in Vocation (B. Voc.)

Major Discipline:	Electronics and Telecommunication Engineering
Years of Study:	03 Years
Semesters:	1, 2, 3, 4, 5, 6
Credits:	130
Additional Requirements:	08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major during Summer Vacation after 3rd Year

Level 6: B.Tech. in Technology with Multidisciplinary Minor

Major Discipline:	Electronics and Telecommunication Engineering
Offered Multidisciplinary Minors:	• Innovation and Entrepreneurship • Biotechnology • IoT and Cloud Computing • Geographical Information System • VLSI • Artificial Intelligence
Years of Study:	04 Years
Semesters:	**Major –** 1, 2, 3, 4, 5, 6, 7, 8 **Multidisciplinary Minors** – 4, 5, 6
Credits:	174

Level 6: B.Tech. in Technology - Honors and Multidisciplinary Minor

Major Discipline:	Electronics and Telecommunication Engineering
Offered Honors and Multidisciplinary Minors:	**Honors:** • Internet of Things* • Artificial Intelligence & Machine Learning • Cyber Security • Virtual and Augmented Reality • Data Science • Blockchain **Multidisciplinary Minors:** • Innovation and Entrepreneurship • Biotechnology • IoT and Cloud Computing* • Geographical Information System • VLSI • Artificial Intelligence * Can be chosen for either Honors or Minors, not both
Years of Study:	04 Years
Semesters:	**Major –** 1, 2, 3, 4, 5, 6, 7, 8 **Multidisciplinary Minors** – 4, 5, 6 **Honors** – 5, 6, 7, 8
Credits:	192 (= Major with Multidisciplinary Minors: 174 + Honors: 18)

Level 6: B.Tech. in Technology - Honors with Research and Multidisciplinary Minor

Major Discipline:	Electronics and Telecommunication Engineering
Offered Multidisciplinary Minors:	• Innovation and Entrepreneurship • Biotechnology • IoT and Cloud Computing • Geographical Information System • VLSI • Artificial Intelligence
Years of Study:	04 Years
Semesters:	**Major –** 1, 2, 3, 4, 5, 6, 7, 8 **Multidisciplinary Minors** – 4, 5, 6 **Honors with Research** – 7, 8
Credits:	192 (= Major with Multidisciplinary Minors: 174 + Honors with Research: 18)

Level 6: B.Tech. in Technology with Double Minors (Multidisciplinary & Specialization)

Major Discipline:	Electronics and Telecommunication Engineering
Offered Multidisciplinary Minors and Specialization Minors:	**Multidisciplinary Minors:** • Innovation and Entrepreneurship • Biotechnology • IoT and Cloud Computing • Geographical Information System • VLSI • Artificial Intelligence **Specialization Minors:** 06 additional courses (of minimum 12 week each), in another Engg. / Tech. discipline / Emerging Areas through MOOC
Years of Study:	04 Years
Semesters:	**Major –** 1, 2, 3, 4, 5, 6, 7, 8 **Multidisciplinary Minors** – 4, 5, 6 **Specialization Minors** – 3, 4, 5, 6, 7, 8
Credits:	192 (= Major with Multidisciplinary Minors: 174 + Specialization Minors: 18)

Credit Distribution Structure for Four Year Multidisciplinary B.Tech. Degree Program in Electronics and Telecommunication Engineering with Multiple Entry Multiple Exit Options

Level	Semester	Faculty: Science and Technology					Faculty: Any	Vocational Skills (VS) & Skill Enhancement (SE) Courses		Ability Enhancement (AE), Indian Knowledge System (IKS), Value Education (VE) Courses			Field Projects / Community Engagement (CE) Projects, Internship (INT), and Co-curricular (CC) Courses			Credits	Cumulative Credits
		Basic Science (BS) Courses	Engineering Science (ES) Courses	Major / Professional Core (PC) Courses	Major / Professional Elective - Department-level (PE-DLC) Courses	Multi-disciplinary Minor (MM) Courses	Open Elective - Institute-level (OE-ILC) Courses	VS - SAT Courses	SE - SAT Courses	AE - SAT Courses	IKS - SAT Courses	VE - SAT Courses	CE - Project-Based Learning (PBL)	INT	CC - SAT Courses		
Level 4.5	I	9	8					1				1			2	21	42
	II	9	8					1		2	1					21	
Exit Option with UG Certificate in Technology with Additional 08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major																	
Level 5.0	III	4		15					1				1			21	85
	IV	4		11		4			1	1			1			22	
Exit Option with UG Diploma in Technology with Additional 08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major																	
Level 5.5	V			11	4	3			1			2	1			22	130
	VI			8	4	3	3	2					3			23	
Exit Option with Bachelor's Degree in Vocation (B. Voc.) with Additional 08 Credit Bridge Course Corresponding to Skill-Based Courses / Internship / Mini Projects in Major																	
Level 6.0	VII			8	7		3						6			24	174
	VIII			8										12		20	
Total		**26**	**16**	**61**	**15**	**10**	**6**	**4**	**3**	**3**	**1**	**3**	**12**	**12**	**2**	**174**	

Program Structure for Third Year UG Technology (EX)

SEMESTER V

TEACHING SCHEME

Course Code	Course Name	Teaching Scheme (Contact Hours)		Credits Assigned		Course Category
		TH – P – TUT	Total	TH – P – TUT	Total	
EXC501	Digital VLSI Design	3 – 0 – 0	03	3 – 0 – 0	03	PC
EXC502	Discrete Time Signal Processing	3 – 0 – 0	03	3 – 0 – 0	03	PC
EXC503	Computer Communication Networks	3 – 0 – 0	03	3 – 0 – 0	03	PC
EXDLC504	Major / Professional Elective – Department-level Course – I	3 – 0 – 0	03	3 – 0 – 0	03	PE-DLC
MMC505	Multidisciplinary Minor Course	3 – 0 – 0	03	3 – 0 – 0	03	MM
EXL501	Digital VLSI Design Laboratory	0 – 2 – 0	02	0 – 1 – 0	01	PC
EXL502	Discrete Time Signal Processing Laboratory	0 – 2 – 0	02	0 – 1 – 0	01	PC
EXDLL504	Major / Professional Elective – Department-level Lab – I	0 – 2 – 0	02	0 – 1 – 0	01	PE-DLC
EXPR54	Community Engagement PBL – Minor Project **(Embedded Systems based projects)**	0 – 2 – 0	02[$]	0 – 1 – 0	01	PBL
EXXS510	Skill Enhancement – SAT X: Skill-Based Learning **(Aptitude/Logic Building and Competitive Programming skills)**	0 – 2[*] – 0	02	0 – 1 – 0	01	SE-SAT
EXXA511	Value Education – SAT XI: Activity - Based Learning **(Business Communication & Ethics)**	0 – 4[**] – 0	04	0 – 2 – 0	02	VE-SAT
Total		**15 – 14 – 0**	**29**	**15 – 7 – 0**	**22**	

[*]SAT can be conducted as TH or P or both as required.

[$]Load of learner, not the faculty.

[**]02 Hours class-wise and 02 Hours batch-wise.

Major /Professional Electives - Department Level Elective Courses and Labs (PE-DLC – I)

	Course Code	Course Title and Group
Major / Professional Elective - Department-level Course – I	EXDLC5041	Group A: Data Compression & Encryption
	EXDLC5042	Group B: Sensor Technology
	EXDLC5043	Group C: Microelectronics Devices and Circuit
	EXDLC5044	Group D: Data Structure and Algorithms

Multidisciplinary Minor Course

	Course	Course Code	Course Title
Multidisciplinary Minor Course	Innovation and Entrepreneurship	MMIEC505	Business Model Development and Prototyping
	Biotechnology	MMBTC505	Genetic Engineering & Omics
	IoT and Cloud Computing	MMICCC505	Cloud Computing for IoT
	Geographical Information Systems	MMGISC505	Remote Sensing and Technology
	Very Large Scale Integration	MMVLSIC505	Analog and mixed-signal IP Design
	Artificial Intelligence	MMAIC505	Artificial Intelligence

SEMESTER V

EXAMINATION SCHEME

Course Code	Course Name	CA Marks			ESE		TW / O / P Marks				Total Marks
		T1	T2	T = T1 + T2	Marks	Duration (in Hrs)	TW	O	P	P&O	
EXC501	Digital VLSI Design	20	20	40	60	2.5	-	-	-	-	100
EXC502	Discrete Time Signal Processing	20	20	40	60	2.5	-	-	-	-	100
EXC503	Computer Communication Networks	20	20	40	60	2.5	-	-	-	-	100
EXDLC504	Major / Professional Elective - Department-level Course – I	20	20	40	60	2.5	-	-	-	-	100
MMC505	Multidisciplinary Minor Course	-	-	-	-	-	50	50	-	-	100
EXL501	Digital VLSI Design Laboratory	-	-	-	-	-	25	-	25	-	50
EXL502	Discrete Time Signal Processing Laboratory	-	-	-	-	-	25	-	-	-	25
EXDLL504	Major / Professional Elective - Department-level Lab – I	-	-	-	-	-	25	-	-	-	25
EXPR54	Community Engagement PBL – Minor Project **(Embedded Systems based projects)**	-	-	-	-	-	25	-	-	25	50
EXXS510	Skill Enhancement -SAT X: Skill-Based Learning (**Aptitude/Logic Building and Competitive Programming skills)**	-	-	-	-	-	25	-	-	-	25
EXXA511	Value Education – SAT XI: Activity - Based Learning (**Business Communication & Ethics)**	-	-	-	-	-	25	25	-	-	50
Total		**80**	**80**	**160**	**240**	**-**	**200**	**75**	**25**	**25**	**725**

Course Code	Course Name	Credits (TH+P+TUT)
EXC501	**Digital VLSI Design**	**3+0+0**
Prerequisite:	1. Electronics Devices & Linear Integrated Circuits 2. Digital Logic Design	
Course Objectives:	1. To introduce process flow of VLSI Design 2. To understand MOSFET operation from VLSI design perspective 3. To learn VLSI design performance metric and trade-offs 4. To design, implement and verify combinational and sequential logic circuits using various MOS design styles 5. To provide an exposure to RTL design	
Course Outcomes:	1. Explain various tools and processes used in VLSI Design 2. Derive expressions for performance parameters of basic building blocks like CMOS inverter 3. Design and realize various combinational and sequential circuits for given specifications 4. Explain working of building blocks of semiconductor memory 5. Illustrate various data path circuits and the issues related to the design of the VLSI system 6. Design digital systems using RTL design technique	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Review of MOSFET operation and Fabrication	1.1 MOSFET structure and operation, IV characteristics, MOSFET Capacitances, MOSFET scaling	1	02	05
	1.2 Overview of VLSI Design Flow, Fabrication process flow of NMOS and CMOS, Lambda based design rules, Stick diagram and mask layout		03	
2. Combinational CMOS Logic Circuits	2.1 CMOS inverter operation, Voltage Transfer characteristics (VTC), Noise Margins, Propagation Delay, Power Dissipation, Design of CMOS Inverter, Layout of CMOS Inverter	2	03	06
	2.2 Realization of CMOS NAND gate, NOR gate, Complex CMOS Logic Circuits, Layout of CMOS NAND, NOR and complex CMOS circuits		03	
3. MOS Design Logic Styles	3.1 Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS,	3	04	08

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Dynamic CMOS Logic, Domino Logic, NORA, Zipper, C^2MOS			
	3.2 Combinational circuit design: MUX, Decoder using above design styles ,1-bit full adder. Concepts of Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS –JK Flip Flop, Edge triggered D-Flip Flop, Realization of Shift Register using design styles		04	
4. Semiconductor Memories	4.1 ROM array, 6T-SRAM (operation, design strategy, leakage currents, sense amplifier), layout of SRAM	4	04	07
	4.2 Operation of 1T and 3T DRAM Cell, NAND and NOR flash memory		03	
5. Data path and system design issues	5.1 Ripple carry adder, CLA adder, carry save adder, carry select adder, carry skip adder, Array Multiplier, Barrel shifter	5	03	09
	5.2 On chip clock generation and distribution, Interconnect delay model, interconnect scaling and crosstalk		02	
	5.3 Design for testability: Fault Types and models, Controllability and observability, Ad hoc testable design techniques, Scan based techniques, Built-in-self-test, Current monitoring test		04	
6. RTL Design	6.1 High Level state machines, RTL design process RTL design of Soda dispenser machine, Laser Based Distance Measurer, FIR Filter	6	04	04
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. CMOS Digital Integrated Circuits Analysis and Design, Third edition, Sung-Mo Kang and Yusuf Leblebici, McGraw Hill, 2012 2. Digital Integrated Circuits: A Design Perspective, Second edition, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson Education, 2013 3. Digital Design with RTL design, VHDL and VERILOG, Second edition, Frank Vahid, John Wiley and Sons Publisher, 2010
Reference Books	1. VLSI Design: A Circuits and Systems Perspective, Third Edition, Neil H. E. Weste, David Harris and Ayan Banerjee, Pearson Education, 2012 2. Introduction to VLSI Circuits and Systems, Student Edition, John P. Uyemura, Wiley, 2013 3. CMOS Circuit Design, Layout and Simulation, Second Edition, R. Jacob Baker, Willey, 2002
Useful Links:	
1. https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ee25/ 2. https://nptel.ac.in/courses/108/103/108103108/ 3. http://cmosedu.com/	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

Two class tests of 20 marks each should be conducted in a semester. The first-class test is to be conducted when approx. 40% syllabus is completed and second-class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour. Addition of both test scores will be considered for passing

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (TH+P+TUT)
EXC502	Discrete Time Signal Processing	3+0+0

Prerequisite:	Signals & Systems
Course Objectives:	1. To develop a thorough understanding of Discrete Fourier transform and its use in frequency domain filter designing 2. To design and realize IIR filters and FIR filters, gain an appreciation for the trade-offs necessary in the filter design and to evaluate the effects of finite word lengths on the filters. 3. To introduce applications of digital signal processing in the field of biomedical and speech signal processing
Course Outcomes:	1. Identify different types of filters based on pass band of given transfer function 2. Illustrate the concepts of Discrete Fourier transform, Fast Fourier transform and apply in system analysis 3. Design digital IIR and FIR filters to satisfy the given specifications and evaluate the frequency response 4. Apply Digital FIR and IIR filter to realize structures 5. Interpret Finite word length Effect in Digital filter 6. Apply signal processing concepts, algorithms in applications related to the field of biomedical and speech signal processing

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Transform Analysis of Linear Time Invariant System	1.1 LTI systems as frequency-selective filters like low pass, high pass, band pass, Notch, comb, all-Pass filters	1	03	05
	1.2 Invertibility of LTI systems, minimum-phase, maximum-phase, mixed-phase system		02	
2. The Discrete Fourier Transform and Efficient Computation	2.1 Relation between DTFT and DFT, Definition and Properties of Discrete Fourier transform (DFT), Inverse DFT, Circular convolution of sequences using DFT and IDFT	2	04	10
	2.2 Linear filtering Technique based on DFT: Evaluation of Linear filtering using DFT, Linear filtering of long data sequences: overlap add and overlap save method		02	
	2.3 Fast Fourier Transform: Radix-2 Decimation in time and Decimation in frequency FFT algorithm and its Inverse, Introduction to Composite -Radix Fast Fourier Transform (FFT)		04	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
3. Design of Digital Filters and Implementation	3.1 Concepts of Infinite Impulse Response (IIR) filter, Mapping of S-plane to Z-plane, Design of Infinite Impulse Response (IIR) filters using Impulse Invariant Method and Bilinear transformation Method from analog filter with examples, Design of Digital Low pass and high pass Butterworth and Chebyshev-I filter from analog filter with examples	3	06	10
	3.2 Concepts of Finite Impulse Response (FIR) filter, Symmetric and Anti-symmetric FIR filter, Design Techniques of FIR filter using various window: Rectangular window, Hamming window, Gibb's phenomenon, Comparison of IIR and FIR filter		04	
4. Digital filter structure	4.1 Realization structures for FIR systems: Cascade form, Frequency sampling structure, Lattice structure, Computational complexities for N length filter	4	03	05
	4.2 Realization structures for IIR systems: Cascade form and parallel form structures, Lattice Ladder structure, Computational complexities for N order filter	5	02	
5. Finite word length Effect in Digital filter	5.1 Quantization Noise, Truncation and Rounding, Effect due to Truncation and Rounding, Coefficient quantization error	5	02	04
	5.2 Dead band, Zero input Limit cycle oscillations and Overflow Limit cycle oscillations		02	
6. Applications of Digital Signal Processing	6.1 Voice Processing, Digital Representation of speech signal, Short Time Spectral Analysis of Speech signal, channel Vocoder, Sub-band Coding, Voice privacy system.	6	03	05
	6.2 Applications of DSP for ECG signal analysis		01	
	6.3 Applications of DSP for Dual Tone Multi-Frequency Signal Detection		01	
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Proakis J., Manolakis D., "*Digital Signal Processing*", 4th Edition, Pearson Education 2. Emmanuel C. Ifeachor, Barrie W. Jervis," Digital Signal Processing", A Practical Approach", Pearson Education 3. A Nagoor Kani "Digital Signal Processing", 2nd Edition. Tata Mc Graw Hill Education Private Limited
Reference Books	1. Sanjit K. Mitra, "Digital Signal Processing – A Computer Based Approach", 4th Edition McGraw Hill Education (India) Private Limited, 2013 2. Oppenheim A., Schafer R., Buck J., "Discrete Time Signal Processing", 2nd Edition, Pearson Education, 3rd Edition, 2010 3. L. R. Rabiner and B. Gold, "Theory and Applications of Digital Signal Processing", PrenticeHall of India, 2006 4. S Salivahan, C Gnanapriya, "Digital Signal Processing", Mc Graw Hill Education (India) limited, 4th Edition, 2015 5. Monson H Hayes, "Digital Signal Processing", Schaum's Outline Series, 2nd Edition, 2011 6. Rangaraj M. Rangayyan, "Biomedical Signal Analysis- A Case Study Approach", Wiley 2002
Useful Links:	
1. Course: Digital Signal Processing By Prof. S.C Dutta Roy, IIT Delhi http://www.nptelvideos.in/2012/12/digital-signal-processing.html 2. Course: Digital Signal Processing By Prof. V. M. Gadre , IIT Bombay https://nptel.ac.in/courses/108/101/108101174/ 3. Course: Digital Signal Processing By Prof. T. K. Basu , IIT Kharagpur https://nptel.ac.in/courses/108/105/108105055/	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

Two class tests of 20 marks each should be conducted in a semester. The first-class test is to be conducted when approx. 40% syllabus is completed and second-class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour. Addition of both test scores will be considered for passing

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (TH+P+TUT)
EXC503	**Computer Communication Networks**	**3+0+0**

Prerequisite:	Analog and Digital Communication Engineering
Course Objectives:	1. To introduce networking architecture and protocols. 2. To understand and recognize the layer wise functions, services, data formats, protocols, hardware devices and addresses in the TCP/IP architecture. 3. To build an understanding of application layer protocols. 4. To apply different addressing and routing schemes.
Course Outcomes:	1. Discuss network topologies, hardware devices, addressing schemes and the protocol stacks. 2. Compare various transmission media and broadband technologies. 3. Analyze the flow control, error control and the medium access control techniques. 4. Analyze network layer addressing and routing schemes. 5. Compare connection oriented and connectionless services. 6. Explore application layer protocols.

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Introduction to Network Architectures, Protocol Layers, and Service models	1.1. Applications of computer networks. Network types: LAN, MAN, and WAN, Network topologies.	1	01	06
	1.2.Protocols and standards, need of layered protocol architecture, OSI reference model.	1	01	
	1.3.TCP/IP architecture: protocol suite, comparison of OSI and TCP/IP	1	01	
	1.4. Layer wise network hardware devices (NIC, Repeaters, Hubs, Bridges, Switches, Routers, Gateway and their comparison)	1	02	
	1.5. Addressing: physical / logical /port addressing/socket addressing.	1	01	
2. Physical Layer	2.1 Guided transmission media: comparison among coaxial, optical fiber and twisted pair cables.	2	01	04
	2.2 Unguided transmission media	2	01	
	2.3 Transmission impairments	2	01	
	2.3 Broadband standards: Cable modem, DSL, and HFC	2	01	
3. Data Link Layer	3.1 Data link services: Framing, Flow control, Error control	3	01	09

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	3.2 ARQ methods: transmission efficiency, Piggybacking	3	03	
	3.3 High Level Data Link Control (HDLC): HDLC configurations, Frame formats, HDLC bit stuffing and de-stuffing, Typical frame exchanges.	3	02	
	3.4 Medium Access Control Protocols: ALOHA, Slotted ALOHA, CSMA, CSMA/CD	3	03	
4. Network Layer	4.1. Introduction to telephone networks and circuit switching principles, Introduction to data networks and packet switching principles, Routing in Packet Switching Networks: Characteristics, Routing strategies, Network layer services and functions.	4	02	12
	4.2. Internet Protocol: Principles of Internetworking, requirements, IPv4 packet, IPv4 addressing (classful and classless (CIDR)), IPv6 (IPv6 Datagram format, comparison with IPv4, and transition from IPv4 to IPv6).	4	03	
	4.3. Routing algorithms: Link state Routing, Distance vector Routing and Path vector routing, Routing protocols: RIP, OSPF, BGP and EIGRP.	4	04	
	4.4. Subnetting, Supernetting, VLSM, and NAT	4	01	
	4.5. Introduction to ICMP, ARP, RARP	4	01	
	4.6. Quality of service	4	01	
5. Transport Layer	5.1. Connectionless and Connection–oriented services at transport layer, Transmission Control Protocol (TCP): TCP Services, TCP Segment, TCP three way handshake	5	03	06
	5.2. User datagram Protocol (UDP), UDP Services, UDP Datagram	5	01	
	5.3. TCP and UDP checksum calculation	5	01	
	5.4. Flow control, error control and congestion control	5	01	
6. Application Layer	Introduction to Application layer Protocols: HTTP, FTP, DNS, SMTP, TELNET, SSH, DHCP.	6	02	02
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Data Communications and Networking, Behrouz A. Forouzan, TMH, 5th Edition, 2013 2. Computer Networks, Andrew S Tanenbaum, Pearson Education, 5th Edition, 2013 3. Computer Networking: A Top-Down Approach, J. J. F. Kurose and K. W. Ross, Addison Wesley, 5th Edition, 2010
Reference Books	1. Communication Networks, Alberto Leon Garcia, McGraw Hill Education, 2nd &4th edition, 2008 2. An Engineering Approach to Computer Networks, S. Keshav, Pearson Education, 2nd Edition, 2015 3. Understanding communications and Networks, W. A. Shay, Cengage Learning, 3rd Edition, 2008 4. Data and Computer Communications, William Stallings, Pearson Education, 10th Edition, 2014
Useful Links:	
NPTEL course videos on Computer Networks and Internet Protocol- https://nptel.ac.in/courses/106/105/106105183/	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

Two class tests of 20 marks each should be conducted in a semester. The first-class test is to be conducted when approx. 40% syllabus is completed and second-class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour. Addition of both test scores will be considered for passing

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Major/Professional Electives – Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5041	**Data Compression and Encryption**	**3+0+0**

Prerequisite:	Applications of Mathematics in Engineering-I
Course Objectives:	1. To understand data compression methods for text, images, video and audio. 2. To study different source coding techniques of data compression. 3. To understand the concepts of cryptography and different algorithms to provide system security 4. To learn to apply different cryptographic techniques
Course Outcomes:	1. Apply different compression techniques on text 2. Explain different data compression methods and standards 3. Explain symmetric and asymmetric cryptography techniques and standards 4. Apply different ciphers and number theory concepts and algorithms to solve the cryptographic problems 5. Describe methods that provide integrity, confidentiality and authentication 6. Describe system security facilities designed to protect the system from security threats

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Introduction to Data Compression	1.1 Data compression, modelling and coding, Lossless and Lossy Compression, Arithmetic Coding – Decoding, Dictionary Based Compression, Sliding Window Compression: LZ-77, LZ-78, LZW	1	05	08
	1.2 Image Compression: DCT, JPEG, JPEG – LS, Differential Lossless Compression, DPCM, JPEG – 2000 Standards	2	03	
2. Video and Audio Compression	2.1 Video compression: Motion compensation, temporal and spatial prediction, MPEG-4, H.264 encoder and decoder.	2	03	06
	2.2 Sound, Digital Audio, μ-Law and A-Law Companding, MPEG –4 Audio Layer, Advanced Audio Coding (AAC) standard		03	
3. Data Security	3.1 Security Goals, Cryptographic Attacks and Techniques	3	02	09
	3.2 Symmetric Key: Substitution Cipher, Transposition Cipher , Stream and Block Cipher		05	
	3.3 DES, double DES and triple DES, AES		02	
4. Number Theory	4.1 Prime Numbers, Fermat's and Euler's Theorem	4	02	04

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	4.2 Chinese Remainder Theorem		02	
5. Asymmetric Key Cryptography	5.1 Principles of Public Key Crypto System, RSA, Key Management, Deffie-Hellman Key Exchange	5	04	08
	5.2 Message Integrity, Message Authentication and Hash Functions, SHA, HMAC, Digital Signature Standards		04	
6. System Security	6.1 Intrusion Detection System, Secure Electronic Transactions	6	02	04
	6.2 Firewall Design, Digital Immune systems, Biometric Authentication, Ethical Hacking		02	
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Khalid Sayood, 3rd Edition, Introduction to Data Compression, Morgan Kauffman 2. Mark Nelson, Jean-Loup Gailly, The Data Compression Book, 2nd edition, BPB Publications 3. William Stallings, Cryptography and Network Security Principles and Practices 5th Edition, Pearson Education. 4. Behrouz A. Forouzan, Cryptography and Network Security, Tata McGraw-Hill.
Reference Books	1. David Salomon, Data Compression: The Complete Reference, Springer 2. Matt Bishop, Computer Security Art and Science, Addison-Wesley 3. Bernard Menesez, Network Security and Cryptography, Delmar Cengage Learning, 7th Edition
Useful Links:	

1. http://www.nptelvideos.com/video.php?id=989
2. https://www.coursera.org/lecture/algorithms-part2/introduction-to-data-compression-OtmHU
3. https://nptel.ac.in/courses/106102064/19
4. 4.https://www.coursera.org/learn/crypto?_escaped_fragment_=&trk=profile_certification_title
5. https://onlinecourses.nptel.ac.in/noc21_cs16/preview/

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

Two class tests of 20 marks each should be conducted in a semester. The first-class test is to be conducted when approx. 40% syllabus is completed and second-class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour. Addition of both test scores will be considered for passing.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Major/Professional Electives – Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5042	**Sensor Technology**	**3+0+0**
Prerequisite:	Electronics Devices and Linear Integrated Circuits	
Course Objectives:	1. To explain basics of sensing techniques and parameters 2. To familiarize about MEMS sensors and Actuators 3. To provide exposure to wireless sensing technologies using sensors and signal conditioning. 4. To provide insight into various sensor applications	
Course Outcomes:	1. Describe the transduction principle of various sensors. 2. Select sensors suitable for required application 3. Analyse wireless sensing techniques 4. Identify signal conditioning method for particular application 5. Design the data acquisition system 6. Implement applications using various sensor technologies	

Module No.	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Introduction	1.1 Classification of Sensors: The sensors are classified with criteria like primary physical quantity to be sensed, transduction principle, material and technology used and application	1	01	03
	1.2 Criteria to choose a Sensor: Accuracy, Precision, Resolution, Environmental condition, Range, Calibration, and Cost		01	
	1.3 Smart Sensors: Low-power, Self –diagnostic and Self- calibration		01	
2. Types of Sensors	2.1 Temperature Sensors: RTD, Thermocouple and Thermistors sensor	2	02	09
	2.2 Proximity Sensors: Inductive (LVDT), Capacitive, Photoelectric and Ultrasonic sensors		02	
	2.3 Chemical Sensors: Gas, Smoke, Conductivity and pH sensor		02	
	2.4 Other Sensors: Optical, Infrared (IR), Sound, Motion, Pressure, Level, Moisture, Humidity, Laser, UV sensors, Ac, IR and Segmented Sensors.		03	
3. MEMS Sensors and Actuators	3.1 MEMS Sensors: General design methodology, techniques for sensing, Pressure sensor , Acceleration sensor, Accelerometers, Angular	2	03	06

Module No.	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Rate sensor and Gyroscopes, Micro machined microphones, Chemical sensors			
	3.2 MEMS Actuators: Techniques for actuation, Digital Micro mirror Device, Micro Machined Valves, Microfluid Devices, IEEE P1451 standard		03	
4. Wireless Sensing Technologies	4.1 Bluetooth: Concepts of Pico net, Scatter net, Link types. Application of Blue tooth with Sensors. IEEE P1451standard	3	02	05
	4.2 ZigBee: components, architecture PLE, Self-Organizing networks and Applications with Sensors		01	
	4.3 Near Field Communication (NFC) and RFID: technical requirements, components and characteristics and their applications with Sensors		02	
5. Data Acquisition and Signal Conditioning	5.1 Signal Conditioning: Block Diagram of Signal Conditioning System, ADC, R2R DAC, Instrumentation Amplifier, Supervisory System (SCADA)	4	02	08
	5.2 Fundamentals of Data Acquisition: Analog and Digital data acquisition system with different configurations, Data loggers, Noise and interference	5	03	
	5.3 Utilization of Signal conditioning circuits for Temperature, Pressure, Optical, Strain gauges, Displacement and Piezoelectric Transducers		03	
6. Sensor Applications	6.1 On-board Automobile sensing system, Home appliances sensors, Aerospace Sensors, Sensors for Environmental Monitoring, Biomedical Sensing Applications.	6	04	08
	6.2 Radio sensors for industrial applications, Remote Sensing, Ground Penetrating Radars, Underwater sensing, Agricultural Sensor applications.		04	
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. An Introduction to Micro electromechanical Systems Engineering, 1st Edition, Nadim Maluf, Kirt Williams, Artech House 2004 2. Micro Electro Mechanical System Design, 2nd Edition, James J. Allen, Taylor and Francis, 2005 3. A Course in Electrical and Electronic Measurements and Instrumentation, 19th Edition, A K Swahney, Dhanpatrai & Co., 2011 4. Instrumentation Devices and System, 2nd Edition, Rangan, Mani and Sharma, Tata McGraw-Hill Publications, 1997
Reference Books	1. Sensors, Actuators and their Interfaces: A Multidisciplinary Introduction, 3rd Edition, Nathan Ida Wiley, 2010 2. Handbook of Modern Sensors Physics, Designs, and Applications, 4th Edition, Jacob Fraden Springer, 2010
Useful Links:	
1. https://nptel.ac.in/courses/108/108/108108147/ 2. https://www.youtube.com/watch?v=vjhp0zTXEsc 3. http://nptel.ac.in/courses/112103174/3	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

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End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Major/Professional Electives – Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5043	**Microelectronics Devices and Circuits**	**3+0+0**
Prerequisite:	1. Electronic Devices and Linear Integrated Circuits 2. Electrical Network Theory	
Course Objectives:	1. To give exposure to MOSFET devices and issues related to it. 2. To introduce Analog integrated circuits based on MOSFET 3. To give exposure to Analog IC design issues 4. To introduce Novel devices and circuits	
Course Outcomes:	1. Explain Model of FET devices 2. Analyze advanced amplifier circuit 3. Evaluate circuit parameter of given circuit 4. Design amplifier circuit for given overheads. 5. Explain working Novel devices and circuit 6. Evaluate capacitance and other physical parameter from Layout of simple integrated circuits	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. MOSFET and scaling	1.1 MOS capacitor CV characteristic and concept of accumulation, depletion and inversion; MOSFET characteristics and SPICE models, Long channel and short channel MOSFET , Short channel effects	1	03	06
	1.2 Transistors along with mask layout diagram, Multi finger transistor, Scaling of MOSFET, CMOS technology	1,6	03	
2. Current Mirror and DC analysis	2.1 Current Mirror, cascade current source, Wilson current source, bias independent current source using MOSFET	2,3	02	06
	2.2 DC analysis and small signal analysis of MOS active load, Differential pair, DC analysis and small signal analysis of MOS advanced active load amplifier, Differential pair	3,4	04	
3. Amplifier with Active loads	3.1 CS amplifier with current source load, CS amplifier with diode connected load, CS amplifier with current source load, Common gate circuit	2,4	03	07
	3.2 Differential pair, Cascode amplifier, Double Cascoding, Folded Cascod	2,3	04	
4. Frequency Response	4.1 Poles and Zeros of CS amplifier, Miller's Theorem, Direct analysis technique, impedance vs frequency	2	04	07

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	4.2 Frequency response of single stage (CS, CG) amplifier. cascode stage, differential stage	2, 4,6	03	
5. Feedback in Circuits	5.1 Loop gain, feedback characteristic, Positive feedback, oscillator Barkhausen's criteria and oscillator example	5	02	07
	5.2 Negative feedback topology: voltage-voltage, voltage-current, current-current, current-voltage fed	3	03	
	5.3 Problem of instability in circuit, Stability analysis of Cascode circuit, Frequency Compensation, miller compensation	3,4	02	
6. Introduction of Novel Devices and circuit Design	6.1 Introduction to FinFet, GAA FETS, double gate, SOI multigate Mosfet	1, 5,6	02	06
	6.2 Analog Design: Device figure of merit, technology issue in circuit design, Flicker noise, matching behaviour and techniques, Layout rules for transistor matching		04	
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. D. A. Neamen, "Electronic Circuit Analysis and Design," Tata McGraw Hill, 2nd Edition 2. A. S. Sedra, K. C. Smith, and A. N. Chandorkar, "Microelectronic Circuits Theory and Applications," International Version, OXFORD International Students, 6th Edition 3. Behzad Razavi, Microelectronics, 2nd Edition
Reference Books	1. Behzad Razavi, Analog Circuit Design, 2nd Edition 2. J.P. Coligne Finfet and other Multi-Gate Transistors
Useful Links:	
1. https://www.semiconductors.org/semiconductors-101/what-is-a-semiconductor/ 2. https://onlinecourses.nptel.ac.in/noc21_ee51/ 3. http://cmosedu.com/	

Continuous Assessment (CA):

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1.	Class Test 1 (T-1)	20 marks
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End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Major/Professional Electives – Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5044	Data Structures and Algorithms	3+0+0

Prerequisite:	Computer Programming
Course Objectives:	1. To introduce the fundamental knowledge & need of Data Structures. 2. To abstract the concept of Algorithm and these concepts are useful in problem solving. 3. To implement fundamental knowledge and applications of Stack, Queue, Linked List, Trees, Graphs etc. 4. To understand the working of different Sorting, Searching & Hashing techniques. 5. To understanding about writing algorithms and step by step approach in solving problems with the help of fundamental data structures. 6. To understand implementation of various strategies like divide and conquer, Dynamic programming.
Course Outcomes:	1. Compare functions using asymptotic analysis and describe the relative merits of worst-, average-, and best-case analysis. 2. Apply various operations on Stack and Queue. 3. Ability to demonstrate the operation of Linked list 4. Ability to demonstrate and apply Trees & Graph data structures. 5. Familiarize with various Sorting- Searching and hashing Algorithms. 6. Ability to analyse different dynamic programming problems.

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Control Structures, Arrays, Recursion, Pointers, Memory Allocation Techniques.	-	02	02
1. Introduction to Data Structures and Algorithms	1.1 Introduction to Data Structures, Concept of ADT, Types of Data Structures: Linear and Nonlinear, Operations on Data Structures.	CO1	02	05
	1.2 Algorithm: Performance characteristics of algorithm, Importance of Algorithm Analysis, Complexity of an Algorithm, Introduction to Asymptotic Analysis and Notations.		03	
2. Stack & Queue	2.1 Introduction to Stack, ADT of Stack, Operations on Stack, Array Implementation of Stack	CO2	2	08
	2.2 Applications of Stack- Infix to Postfix Expression Conversion, Infix Expression to Prefix Expression Conversion, Postfix Expression Evaluation		2	
	2.3 Introduction to Queue, ADT of Queue, Operations on Queue, Array Implementation of Queue, Types of Queue-Circular Queue, Priority Queue, Introduction to Double Ended Queue		3	
	2.4 Applications of various types of Queue		1	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
3. Linked List	3.1 Introduction to Linked list, Linked List v/s Array, Representation of Linked List, Types of Linked List - Singly Linked List, Doubly Linked List.	CO3	2	07
	3.2 Operations on Singly Linked List and Doubly Linked List		2	
	3.3 Singly Linked List Application-Polynomial Representation and Addition, Doubly Linked List Application		3	
4. Trees & Graph	4.1 **Trees:** Introduction, Tree Terminologies, Binary Tree, Binary Tree Representation, Types of Binary Tree, Binary Tree Traversals, Binary Search Tree, Operations on Binary Search Tree,	CO4	2	09
	4.2 Applications of Binary Tree- Expression Tree, Huffman Encoding.		2	
	4.3 **Graph:** Introduction, Graph Terminology, Memory Representation of Graph, Operations Performed on Graph.		2	
	4.4 Graph Traversal, Breadth First Search, Depth First Search, Applications of the Graph, Shortest Path, Minimum Spanning Tree.		3	
5. Searching – Sorting and Hashing Algorithms	5.1 **Searching:** Sequential Search, Index Sequential Search, Binary Search**.**	CO5	2	6
	5.2 **Sorting:** Bubble Sort, Quick Sort, Merge Sort.		2	
	5.3 **Hashing:** Hashing-Concept, Hash Functions, Common hashing functions, Collision resolution Techniques.		2	
6. Dynamic Programming	All pair shortest path (Floyd-Warshall algorithm), Single source shortest path, (Dijkstra's Algorithm), 0/1 knapsack, Travelling salesman problem.	CO6	4	4
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Data Structures A Psedocode Approach with C, Richard F. Gilberg & Behrouz A. Forouzan, Second edition, CENGAGE Learning 2. Data Structures using C, Reema Thareja, Oxford University press 3. Introduction to Data Structure and its Applications Jean-Paul Tremblay, P. G. Sorenson 4. Ellis Horowitz, Sartaj Sahni, S. Rajsekaran. "Fundamentals of computer algorithms" University Press 5. T.H.Coreman , C.E. Leiserson, R.L. Rivest, and C. Stein, "Introduction to algorithms", 2nd edition , PHI publication 2005. 6. Alfred v. Aho, John E. Hopcroft , Jeffrey D. Ullman , "Data structures and Algorithm" Pearson education, Fourth impression 2009
Reference Books	1. Data Structures Using C & C++, Rajesh K. Shukla, Wiley- India 2. Data Structures Using C, ISRD Group, Second Edition, Tata McGraw-Hill 3. Data Structure Using C, Balagurusamy 4. C & Data Structures, Prof. P.S. Deshpande, Prof. O.G. Kakde, Dreamtech press 5. Data Structures, Adapted by: GAV PAI, Schaum's Outlines 6. Michael Gooddrich & Roberto Tammassia, "Algorithm design foundation analysis and internet examples", Second edition , Wiley student edition
Useful Links:	
1. https://learndsa.kjsieit.in/ 2. https://nptel.ac.in/courses/106/102/106102064/ 3. https://www.coursera.org/specializations/data-structures-algorithms 4. https://www.edx.org/course/data-structures-fundamentals 5. https://swayam.gov.in/nd1_noc19_cs67/preview	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	20 marks
2.	Class Test 2 (T-2)	20 marks

Class Tests (20 Marks):

Two class tests of 20 marks each should be conducted in a semester. The first-class test is to be conducted when approx. 40% syllabus is completed and second-class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour. Addition of both test scores will be considered for passing.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (P+TUT)
EXL501	**Digital VLSI Digital Laboratory**	**1 + 0**
Lab Prerequisite:	Digital Logic Design	
Lab Objectives:	1. To simulate the various phenomenon related to CMOS circuits 2. To analyse simple CMOS circuits using SPICE tools 3. To simulate the logic circuits using various design style 4. To draw mask layout of various circuits	
Lab Outcomes:	1. Implement SPICE model for given combinational and sequential CMOS circuits. 2. Perform various analysis like operating point, dc, transient etc. of given CMOS circuits. 3. Design, simulate, and verify CMOS circuit for given specification and Evaluate performance of the same. 4. Draw layout of given CMOS circuit and also able extract various parasitic using open source layout tool like Magic. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.	

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Constant Voltage and Constant field MOSFET scaling	2,5,6	02
2	Layout of MOSFET and extraction of parasitic capacitances	4,5,6	02
3	Voltage transfer characteristics of CMOS inverter and calculation of Noise Margin and static power	2,5,6	02
4	Transient Analysis of CMOS inverter and calculation of t_{pHL}, t_{pLH}, t_r, t_f and average power	3,5,6	02
5	Design of CMOS inverter for given specifications	3,5,6	02
6	Layout of CMOS inverter and comparison of pre layout and post layout performance	4,5,6	02
7	Voltage transfer characteristics of 2 input NAND/NOR gate and calculation of noise margins and validation using equivalent inverter approach	2,5,6	02
8	Transient Analysis of 2 input NAND/NOR CMOS gate and calculation of t_{pHL}, t_{pLH}, t_r, t_f, average power and validation using equivalent inverter approach	3,5,6	02
9	Layout of 2 input CMOS NAND/NOR gate and comparison of pre layout and post layout performance	4,5,6	02
10	Static and transient analysis of Complex CMOS gate	3,5,6	02
11	Layout of complex CMOS gate using Euler path	4,5,6	02
12	Implementation of various combinational and sequential circuits using different design styles	1,5,6	02

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
13	Design and implementation of NAND based and NOR based ROM array	3,5,6	02
14	Performance analysis of 6T-SRAM Cell	3,5,6	02
15	Design of 6T SRAM cell robust read and write operation	3,5,6	02
16	Performance analysis of 1T and 3T DRAM Cell	3,5,6	02
17	RTL design of Soda dispenser machine	1,5,6	02
18	RTL design of FIR Filter	1,5,6	02
		Total	**38***
***Minimum 28 Hrs. Lab / Mini Project to be conducted**			
Virtual Lab Links: https://vlsi-iitg.vlabs.ac.in/			

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/ Case study /Project/ demo/ presentation: 10-marks)

Oral/Practical/P&O:

Practical examination will be based on the experiment list and content of the entire theory syllabus and carries 25-Marks

Course Code	Course Name	Credits (P+TUT)
EXL502	**Discrete Time Signal Processing Laboratory**	**1+0**
Lab Prerequisite:	Signals and Systems	
Lab Objectives:	1. To carry out basic discrete time signal processing operations 2. To implement and design FIR filters and IIR filters 3. To implement applications related to the field of biomedical signal processing and audio signal processing	
Lab Outcomes:	1. Demonstrate their ability to perform frequency analysis of different discrete time sequences. 2. Perform basic signal processing operations such as circular convolution of discrete time sequences. 3. Design and implement IIR & FIR Filters for given specifications. 4. Analyse and Implement applications related to the field of biomedical signal processing and audio signal processing 5. Write accurate Documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.	

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Impulse response of Discrete Time System	1,5,6	02
2	4-point DFT of Discrete Time Sequence	1,5 ,6	02
3	Circular Convolution of Discrete Time Sequence	1,2,5,6	02
4	8- point DFT of Discrete Time Sequence	1,5,6	02
5	Butterworth IIR filter using Impulse Invariance Transformation	3,5,6	02
6	Butterworth IIR filter using Bilinear Transformation Technique	3,5,6	02
7	Chebyshev filter using Bilinear Transformation Technique	3,5,6	02
8	Impulse response of FIR band pass filter	3,5,6	02
9	Impulse FIR filter using Rectangular Window	3,5,6	02
10	Case study on different applications of Digital Signal Processing	4,5,6	08
		Total	**28**

Virtual Lab Links: vlabs.iitkgp.ernet.in/dsp/#
Term work: 1. Term work should consist of a minimum of 8 experiments. 2. Journal must include assignments on content of theory and practical of the course. 3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. 4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	Major/Professional Electives – Department Level Elective Course - I Laboratory	Credits (P+TUT)
EXDLL5041	**Data Compression and Encryption Laboratory**	**1+0**
Lab Prerequisite:	Any suitable programming skills	
Lab Objectives:	1. To apply statistical and dictionary methods for text compression 2. To understand on how to apply the concept of quantization and audio/image compression 3. To understand the concepts of Encryption and techniques of Encryption 4. To understand on how to apply the cryptographic algorithm	
Lab Outcomes:	1. Implement Text compression Techniques 2. Implement Image compression techniques 3. Implement data Encryption technique 4. Implement public key cryptography algorithms 5. Write accurate documentation for experiments performed 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory	

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Write a program to encode and decode message and find code efficiency using Arithmetic Coding	1,5,6	02
2	Write a program to encode and decode the text using Dictionary methods	1,5,6	02
3	Write a program to Discrete Cosine Transform for image compression	2,5,6	02
4	To study DPCM Audio Compression Method	2,5,6	02
5	To study the effect of Uniform and Non uniform Quantization on speech signal	2,5,6	02
6	Write a program to apply Affine Cipher Encoding and decoding for data encryption	3,5,6	02
7	Write a program to apply Caesar Cipher Encoding and decoding for data encryption	3,5,6	02
8	Write a program to implement Diffie-Hellman Public Key Cryptography	4,5,6	02
9	To study RSA Public Key Encryption and Decryption Algorithm	4,5,6	02
10	To study the Message Authentication algorithm	4,5,6	02
11	Case Study / Mini Project	1,2,3,4,5,6	06
		Total	**28**

Virtual Lab Links: 1/cse29-iiith.vlabs.ac.in/
Term work: 1. Term work should consist of a minimum of 8 experiments. 2. Journal must include assignments on content of theory and practical of the course. 3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. 4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	Major/Professional Electives – Department Level Elective Course - I Laboratory	Credits (P+TUT)
EXDLL5042	**Sensor Technology Laboratory**	**1+0**
Lab Prerequisite:	1. Knowledge of implementing Electronic Circuits 2. Interfacing devices for processing such as Arduino, Raspberry Pi, Microprocessors and Microcontrollers. 3. Signal Conditioning Circuits	
Lab Objectives:	1. To implement basic applications using different types of Sensors. 2. To apply the knowledge of MEMS and Smart sensors by implementing applications 3. To implement signal conditioning circuits to shape the input signals. 4. To interface sensors with various communication Technologies	
Lab Outcomes:	1. Develop basic sensor application circuit using sensors like temperature, smoke, humidity, moisture sensors. 2. Apply the smart sensors and connect them to different platforms like wired and wireless. 3. Design suitable signal conditioning to different types of sensor outputs for further processing. 4. Implement applications based on A to D convertors and D to A convertors and connect them to sensor circuits through different case studies. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory	

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Study of different types of sensors by observing them in the lab and study the important parameters like accuracy, Precision, Resolution, Range, tolerance limits etc.	1,5,6	02
2	Implement a circuit to detect smoke.	1,5,6	02
3	Design bimorph cantilever which acts as a pressure sensor.	2,5,6	02
4	Model and simulate Electro-mechanical actuator. Do dc and transient analysis	2,5,6	02
5	Simulate the harvested electrical power from mechanical vibrations using piezoelectric cantilever beam.	2,5,6	02
6	Model and simulate accelerometer	2,5,6	02
7	Implement A to D conversion	3,5,6	02
8	Implement R2R D to A convertors	3,5,6	02
9	Interfacing the Zigbee with humidity sensors.	4,5,6	02
10	Interfacing RFID with proximity sensors	4,5,6	02
11	Study of NFC and suitable sensors for interfacing.	4,5,6	02
12	Case Study / Mini Project	1 to 6	04
		Total	**28**

Virtual Lab Links: https://ssp-iitb.vlabs.ac.in/
Term work: 1. Term work should consist of a minimum of 8 experiments. 2. Journal must include assignments on content of theory and practical of the course. 3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. 4. Total 25 Marks (Experiments: 15-marks, Assignments/ Case study/ Project/ demo/ presentation: 10-marks)

Course Code	Major/Professional Electives – Department Level Elective Course - I Laboratory	Credits (P+TUT)
EXDLL5043	**Microelectronics Devices and Circuits Laboratory**	**1 + 0**

Lab Prerequisite:	Electronic Devices & Linear Integrated Circuits
Lab Objectives:	1. To provide insight into Analog circuit design using CAD tools 2. To gain proficiency in integrated circuit analysis using LTspice 3. To provide exposure to Layout IC design 4. To provide insight into Analog design flow process
Lab Outcomes:	1. Design amplifier circuits in LTspice simulation environment. 2. Design layout of amplifier inverter in Electric 3. Analyse from the data available from simulation in LTspice 4. Asses different circuit and device models 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the Laboratory

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Installations and demonstration of CAD Design software: types, working roles in IC design	5,6	02
2	Plot long and short channel MOSFET characteristics	3,4,5,6	02
3	DC analysis of advance active load amplifier	3,4,5,6	02
4	DC analysis of Cascode amplifier	3,4,5,6	02
5	Transient analysis of Cascode amplifier	3,4,5,6	02
6	AC Analysis of Cascode amplifier	3,4,5,6	02
7	AC analysis of Differential amplifier	3,4,5,6	02
8	CMOS inverter simulation	3,4,5,6	02
9	CMOS inverter Layout simulation, DRC, LVS steps.	2,5,6	02
10	Layout of CS amplifier	2,5,6	02
11	Implement available Compact model equation in octave	3,5,6	02
12	Implementation of CAD Design software using simple techniques/available open source software for mobile devices	5,6	02
13	Study of Verilog-A software and design flow	5,6	02
		Total	**28**

Virtual Lab Links:

1. http://vlabs.iitkgp.ernet.in/be/
2. http://cmosedu.com/
3. https://www.youtube.com/watch?v=rXTEmojksd4

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	Major/Professional Electives – Department Level Elective Course - I Laboratory	Credits (P+TUT)
EXDLL5044	**Data Structures and Algorithm Laboratory**	**1+0**

Lab Prerequisite:	1. Computer Programming 2. Computer Programming Laboratory
Lab Objectives:	1. To implement basic data structures such as linked lists, stacks and queues 2. To solve problem involving graphs and trees 3. To choose appropriate data structure and apply it to various problems
Lab Outcomes:	1. Choose appropriate data structure as applied to specify problem definition and to select appropriate problem solving strategies. 2. Use linear and non-linear data structures like stacks, queues, linked list etc. 3. Calculate time complexity and space complexity of an algorithm. 4. Analyse different divide and conquer problems, dynamic programming problems. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Implementations of stack menu driven program	1,5,6	02
2	* Implementations of Infix to Postfix Transformation and its evaluation program	2,5,6	02
3	Implementations of queue menu driven program	1,5,6	02
4	* Implementations of double ended queue menu driven program	1,2,5,6	02
5	* Implementation of different operations on linked list – copy, concatenate, split, reverse, count no. of nodes etc.	1,2,5,6	02
6	Implementation of polynomials operations (addition, subtraction) using Linked List	2,5,6	02
7	*Implementations of Binary Tree menu driven program	2,5,6	02
8	*Implementation of construction of expression tree using postfix expression.	3,5,6	02
9	* Implementations of Graph menu driven program (DFS & BSF)	3,5,6	02
10	Write a program for a. selection sort b. insertion sort	3,5,6	02
11	* Write a program using Divide and Conquer for a. Merge sort analysis b. Quick sort analysis	4,5,6	02
12	Write a program using Divide and Conquer for a. binary search b. finding minimum and maximum	4,5,6	02

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
13	*Write a program for Optimal binary search tree using dynamic programming	4,5,6	02
14	*Write a program for Travelling salesman problem using dynamic programming	4,5,6	02
		Total	**30**
* Compulsory / **Minimum 28 Hrs. Lab / Mini Project to be conducted**			
Useful Links:			
1. https://www.programiz.com/dsa 2. https://www.codechef.com/certification/data-structures-and-algorithms/prepare			

Term work:

1. Term work should consist of a minimum of 8 experiments
2. Journal must include assignments on content of theory and practical of the course
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/demo/presentation: 10-marks

Course Code	Community Engagement PBL – Minor Project	Credits (TH+P+TUT)
EXPR54	**(Embedded Systems based Projects)**	**0 +1+ 0**
Prerequisite:	1. Microcontrollers 2. Electronic Devices & Linear Integrated Circuits 3. Mini Project 1B: Arduino & Raspberry Pi based Projects	
Minor Project Objectives:	1. To develop background knowledge of Embedded Systems. 2. To understand the design of embedded systems. 3. To choose proper microcontroller for Embedded systems 4. To understand use of wireless sensors/communications with Embedded systems 5. To understand communication techniques. 6. To write programs for embedded systems and real time operating systems / IoT	
Minor Project Outcomes:	1. Outline the embedded systems concept with design metrics 2. Outline microcontroller's concept. 3. Implement the Embedded systems with different sensors and peripherals as IoT. 4. Implement the Embedded systems with different communication protocols as IoT. 5. Analyse concepts of Real time operating systems. 6. Design embedded system applications using sensors, peripherals and RTOS	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Hrs/ Topic
1. Introduction	1.1 Definition of Embedded System, Embedded Systems Vs General Computing Systems, Classification, Major Application Areas. Characteristics and quality attributes (Design Metric) of embedded system	1	02	04
	1.2 Identification of Project Title		02	
2. Controller boards and Programming – Embedded C	2.1 ARM LPC 21XX (2148), STM32 boards and Texas MSP 430 lunchbox/ Tiva C board and PIC/PSoc*	2	01	04
	2.2 Comparison of C and embedded C, Data Types, Variable, Storage Classes, Bit operation, Arrays, Strings, Structure and unions, Classifier		01	
	2.3 Exercise: Identify the suitable board required for the particular application with respect to design metrics. (Hint: check clock frequency (speed), memory (program and data), no. of		01	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Hrs/ Topic
	ports for peripherals, timers/counters and serial communication requirement for project)			
	2.4 Suggested Way to Identify: https://predictabledesigns.com/how-to-selectthe-microcontroller-for-your-new-product/		01	
3. Interfacing Sensors and peripherals using Embedded C	3.1 Sensors and Signal Conditioning Circuits amplifiers /attenuators /filters /comparators/ADC and DAC) , Interfacing with GLCD/TFT display, Relays and Drivers for interfacing Motors (DC and stepper)	3	02	05
	3.2 Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application		01	
	3.3 Study Material: For LCD interfacing with MSP430 Launch Pad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc.		02	
4. Communication with programming in Embedded C	4.1 Serial communication, CAN bus, I2C, MOD bus, SPI	4	01	05
	4.2 Interfacing with Wi-Fi, Bluetooth ,ZigBee, LoRa, RFID and putting data on IoT		01	
	4.3 Interfacing with GSM module , GPS module, SD card		01	
	4.4 Exercise: Understand Communication requirement for selected application and test it		01	
	4.5 STM32:https://controllerstech.com/serial-transmission-in-stm32/#:~:text=Serial%20Transmission%20in%20Stm32&text=UART%20is%20widely%20used%20for,amongst%20which%20communication%20is%20 done. LPC2148: https://www.electronicwings.com/arm7/lpc2148-uart0 MSP430: https://www.ti.com/lit/ml/slap117/slap117.pdf		01	
	5.1 Operating system basics, Types of OS , Tasks, process, Threads	5	02	04

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Hrs/ Topic
5. Real Time Operating Systems [RTOS]	5.2 Multiprocessing and Multitasking, Task scheduling		01	
	5.3 RTLinux/ Free RTOS and Mbed OS, Implementation with RTOS		01	
6. Cloud/ Web server	6.1 Implementation on web server	6	01	04
	6.2 Thingspeak, AWS cloud platform for IoT based programming and modelling		01	
	6.3 Exercise : Perform ESP8266 interface with microcontroller		01	
	6.4 Study Material: STM32: https://circuitdigest.com/microcontroller-projects/interfacingesp8266-with-stm32f103c8-stm32-to-create-a-webserver LPC2148: https://circuitdigest.com/microcontroller-projects/iot-based-ARM7-LPC2148-webserver-to-control-an-led MSP430: https://circuitdigest.com/microcontroller-projects/sending-emailusing-msp430-and-esp8266		01	
			Total	**26**

Books:	
Text Books	1. Shibu K.V," Introduction to Embedded Systems", Mc Graw Hill, 2nd edition. 2. Frank Vahid, and Tony Givargis, "Embedded System Design: A unified Hardware/Software Introduction", Wiley Publication. 3. Raj Kamal," Embedded Systems Architecture, Programming and design", Tata McGraw-Hill Publication. 4. 4. Dr. K.V.K.K. Prasad, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
Reference Books	1. Iyer, Gupta," Embedded real systems Programming", TMH 2. David Simon, "Embedded systems software primer', Pearson 3. Andrew Sloss, Dominic Symes and Chris Wright, "ARM_System_Developers_GuideDesigning_and_Optimizing_System_Software" Elsevier and Morgan Kaufmann Publishers.

Useful Links:

1. Introduction to Embedded System Design (using MSP430) https://onlinecourses.nptel.ac.in/noc20_ee98/preview
2. Embedded System Design with ARM https://onlinecourses.nptel.ac.in/noc20_cs15/preview
3. Embedded systems https://nptel.ac.in/courses/108/102/108102045/
4. Master Microcontroller and Embedded Driver Development (MCU1) STM32 Udemy course link mastering microcontrollers with peripherals
5. Texas Instruments (TI) Trainings: https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2103/training-support
6. Texas Instruments (TI) Teaching material/ text books: https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2035/textbooks

Continuous Assessment: Practical (25 Marks)

A. Guideline of Minor project are as follows :

1. To achieve proper selection of Minor Projects. Students should do a survey of different microcontroller board from given microcontroller series tools and identify which is most suitable for their selected topic. They should consult with their Guide/Mentors / Internal committee to finalize it.
2. Students shall submit implementation plan in the form of Smart Report/Gantt/PERT/CPM chart, which will cover weekly activity of minor project.
3. A logbook to be prepared by each group, wherein group can record weekly work progress. Guide/ supervisor will verify it and will put notes/comments.
4. Guide/supervisor guidance is very much important during minor project activities; however, focus shall be on self-learning.

Suggested steps for Minor project selection and implementation

Minor project should be completely microcontroller based

Follow these steps:

a) Take specification, using these specifications design project.
b) Select proper microcontroller board considering features and requirements of project.
c) Program it using Embedded C and perform verification of each module (sensors/communication protocol)
d) Test Functional Simulation and verify it using simulation tool.
e) Make hardware connection on GPP of peripherals with microcontroller board and execute the program.
f) Troubleshoot if not get expected result.

B. Project Topic selection and approval :

1. The group may be of maximum THREE (03) students.
2. Topic selection and approval by 2 Expert faculties from department at the start of semester.
3. Log Book to be prepared for each group to record the work progress in terms of milestones per week by students. Weekly comment, remarks to be put by guiding faculty. Both students and faculty will put signature in it per week. The log book can be managed online with proper authentication method using Google sheets/forms or open source project management software.

C. Project Report Format:

1. Report should not exceed 30 pages. Simply staple it to discourage use of plastic.
2. Report must contain block diagram, circuit diagram, screenshot of outputs and datasheets of microcontrollers and peripherals (Include only required information pages).
3. The recommended report writing format is in LaTex.(https://youtu.be/YLm3sXlKpHQ)

Term Work: (25 marks)

1. Term Work evaluation and marking scheme:

a. The review/ progress monitoring committee shall be constituted by Head of Departments of each institute.
b. The progress of minor project to be evaluated on continuous basis, minimum two reviews in each semester.
c. At end of semester the above 2 expert faculty who have approved the topic will internally evaluate the performance.
d. Students have to give presentation and demonstration on the Embedded Systems Minor Project at end of semester before submission to above experts.
e. In the evaluation each individual student should be assessed for his/her contribution, understanding and knowledge gained about the task completed. Based upon it the marks will be awarded to student.
f. Distribution of 25 Marks scheme is as follows:
   i. Marks awarded by guide/supervisor based on log book and output: 10
   ii. Marks awarded by review committee: 10
   iii. Quality of Project report: 05

2. Guidelines for Assessment of Minor Project Practical/Oral Examination:

a. Report should be prepared as per the guidelines issued by the University of Mumbai.
b. Minor Project shall be assessed through a presentation and demonstration of working model by the student project group to a panel of Internal and External Examiners preferably from industry or research organisations having experience of more than five years approved by head of Institution.

Text Books:

1.Quantitative abilities by Arun Sharma
2. Quantitative Aptitude for Competitive Examinations by R S Agrawal
3. Verbal and Non-Verbal reasoning by R S Agrawal
4. Guide to Competitive Programming Learning and Improving Algorithms Through Contests Antti Laaksonen, Department of Computer Science, University of Helsinki, Finland

Reference Books:

1. Algorithms Illuminated by Tim Roughgarden
2. Algorithm Design, Jon Kleinberg and Éva Tardos
3. Introduction to Algorithms, Cormen, Leiserson, Rivest, Stein
4. Competitive Programming 4: The Lower Bound of Programming Contests in the 2020s by Steven Halim and Felix Halim
5. Guide to Competitive Programming: Learning and Improving Algorithms Through Contests Antti Laaksonen.

Useful Links:

1. https://doi.org/10.1007/978-3-319-72547-5
2. Algorithms by Jeff Erickson (freely available online)
3. https://onlinecourses.nptel.ac.in/noc21_cs99/preview
4. https://unacademy.com/a/i-p-c-beginner-track

Term Work (25 Marks):

Marks will be awarded based on Assessment Rubrics:

1. Student's active participation in skill based learning.
2. Presenting/showcasing learned skills through Social /outreach/ extension activities/Events/ Competitions/Trainings/Internships etc.
3. Submission of Report/act/demonstrations/ specific participation/Idea creation/scope/creativity/Case study etc.
4. Achievement/Recognition.

Oral/Practical/P&O :

P&O examination will be based on the and carries 25-Marks

Skill Based Learning Code	Skill Enhancement - SAT - X: Skill Based Learning	Credits (TH+P+TUT)
EXXS510	**Aptitude/Logic Building and Competitive Programming skills**	**0+1+0**
Skill Prerequisite	1. Knowledge of elementary mathematics (HSC level) 2. Knowledge of basic English grammar (SSC level) 3. Knowledge of Basic programming languages	

Skill Objectives	1. To have the basic awareness about how to prepare for recruitment process 2. To introduce the students to computational skills required to appear for recruitment tests. 3. To introduce the students to coding skills required to appear for recruitment tests/ project /coding competitions.

Skill Outcomes	1. Discuss the basic concepts of QUANTITATIVE ABILITY 2. Discuss the basic concepts of LOGICAL REASONING Skills 3. Acquire satisfactory competency in use of VERBAL REASONING 4. Solve campus placements aptitude papers covering Quantitative Ability, Logical Reasoning and Verbal Ability 5. Use most common algorithms for competitive programming 6. Analyse data structures for competitive up solving.

Module No & Name	Sub Topics	SO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
1. Basics of Quantitative Abilities	1.1 Problems on Number System Problems on HCF and LCM Problems on Average	1,4	02	06
	1.2 Problems on Ratio and Proportion, Problems on Percentage		02	
2. Arithmetic Quantitative Abilities	2.1 Problems on Ages, Problems on Profit and Loss	1,4	02	06
	2.2 Problems on Simple and Compound Interest, Problems on Time and Distance		02	
3. Logical Reasoning	3.1 Number Series, Alpha Numerical, Letter & Symbol Series	2,4	02	04
	3.2 Numerical and Alphabet Puzzles, Seating Arrangement			
4. Programming Techniques	4.1 What is Competitive Programming? Programming Contests, Language Features	5	02	05
	4.2 Recursive Algorithms, Bit Manipulation		03	
5. Sorting and Searching	Sorting Algorithms, Solving Problems by sorting, Binary Search	6	05	05

ii. Course Conclusion	Course recap, Outcomes, Discussion	-	-	02
			Total:	**28**

Text Books:

1.Quantitative abilities by Arun Sharma

2. Quantitative Aptitude for Competitive Examinations by R S Agrawal

3. Verbal and Non-Verbal reasoning by R S Agrawal

4. Guide to Competitive Programming Learning and Improving Algorithms Through Contests Antti Laaksonen, Department of Computer Science, University of Helsinki, Finland

Reference Books:

1. Algorithms Illuminated by Tim Roughgarden
2. Algorithm Design, Jon Kleinberg and Éva Tardos
3. Introduction to Algorithms, Cormen, Leiserson, Rivest, Stein
4. Competitive Programming 4: The Lower Bound of Programming Contests in the 2020s by Steven Halim and Felix Halim
5. Guide to Competitive Programming: Learning and Improving Algorithms Through Contests Antti Laaksonen.

Useful Links:

1. https://doi.org/10.1007/978-3-319-72547-5
2. Algorithms by Jeff Erickson (freely available online)
3. https://onlinecourses.nptel.ac.in/noc21_cs99/preview
4. https://unacademy.com/a/i-p-c-beginner-track

Term Work (25 Marks):

Marks will be awarded based on Assessment Rubrics:

1. Student's active participation in skill based learning.
2. Presenting/showcasing learned skills through Social /outreach/ extension activities/Events/ Competitions/Trainings/Internships etc.
3. Submission of Report/act/demonstrations/ specific participation/ Idea creation/scope/creativity/Case study etc.
4. Achievement/Recognition.

Course Code	Value Education – SAT XI: Activity-Based Learning	Credits (TH+P+TUT)
EXXA511	**Business Communication & Ethics**	**0+2+0**
Hardware Requirements:	PC With following Configuration 1. Intel Dual core Processor or higher 2. Minimum 4 GB RAM 3. Minimum 40 GB Hard disk	
Software Requirements:	1. Microsoft Windows 10 Desktop OS 2. Language Laboratory Software: ODLL (Orell Digital Language Laboratory)	
Lab Prerequisite:	Fundamental knowledge of Professional Communication Skills as acquired in semester II	
Course Rationale:	This curriculum is designed to build up a professional and ethical approach, effective oral and written communication with enhanced soft skills. Through practical sessions, it augments student's interactive competence and confidence to respond appropriately and creatively to the implied challenges of the global Industrial and Corporate requirements. It further inculcates the social responsibility of engineers as technical citizens.	
Lab Objectives:	1. To discern and develop an effective style of writing important technical/business documents 2. To investigate possible resources and plan a successful job campaign 3. To comprehend the dynamics of professional communication in the form of group discussions, meetings, etc. required for career enhancement 4. To develop creative and impactful presentation skills 5. To have personal traits, interests, values, aptitudes and skills 6. To understand the importance of integrity and develop a personal code of ethics	
Lab Outcomes:	1. Plan and prepare effective business/ technical documents, which will in turn provide a solid foundation for their future managerial roles. 2. Strategize their personal and professional skills to build a professional image and meet the demands of the industry. 3. Emerge successful in group discussions, meetings and result-oriented agreeable solutions in-group communication situations. 4. Deliver persuasive and professional presentations. 5. Develop creative thinking and interpersonal skills required for effective professional communication 6. Apply codes of ethical conduct, personal integrity and norms of organizational behaviour	

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Advanced Technical Writing: Project/ Problem Based Learning	1.1 Classification of Reports: Classification on the basis of: Subject Matter (Technology, Accounting, Finance, Marketing, etc.) Time Interval (Periodic, One-time, Special) Function (Informational, Analytical, etc.) Physical Factors (Memorandum, Letter, Short & Long)	1, 6	01	06
	1.2 Parts of a Long Formal Report: Prefatory Parts (Front Matter) Report Proper (Main Body) Appended Parts (Back Matter)		01	
	1.3 Language and Style of Reports Tense, Person & Voice of Reports Numbering Style of Chapters, Sections, Figures, Tables and Equations Proofreading through Plagiarism Checkers		01	
	1.4 Definition, Purpose & Types of Proposals Solicited (in conformance with RFP) & Unsolicited Proposals Types (Short and Long proposals)		01	
	1.5 Parts of a Proposal Elements Scope and Limitations Conclusion		01	
	1.6 Technical Paper Writing Parts of a Technical Paper (Abstract, Introduction, Research Methods, Findings and Analysis, Discussion, Limitations, Future Scope and References) Language and Formatting Referencing in IEEE Format		01	
2. Employment Skills	2.1. Cover Letter & Resume Parts and Content of a Cover Letter Difference between Bio-data, Resume & CV Essential Parts of a Resume Types of Resume (Chronological, Functional & Combination)	2, 4	01	06
	2.2 Verbal Aptitude Test Modelled on CAT, GRE, GMAT exams		01	
	2.3 Group Discussions		01	

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Purpose of a GD Parameters of Evaluating a GD			
	Types of GDs (Normal, Case-based & Role Plays)		01	
	GD Etiquettes		01	
	2.4 Personal Interviews Planning and Preparation Types of Questions Types of Interviews (Structured, Stress, Behavioural, Problem Solving & Case-based) Modes of Interviews: Face-to-face (One-to one and Panel) Telephonic, Virtual		01	
3. Business Meetings	3.1 Conducting Business Meetings Types of Meetings Meeting etiquettes		01	02
	3.2 Documentation Notice Agenda Minutes	3, 6	01	
4. Technical/ Business Presentations	4.1 Effective Presentation Strategies Defining Purpose Analyzing Audience, Location and Event Gathering, Selecting & Arranging Material		01	02
	4.2 Structuring a Presentation Making Effective Slides Types of Presentations Aids Closing a Presentation	2, 4	01	
5. Interpersonal Skills	5.1 Emotional Intelligence		01	08
	Motivation		01	
	Assertiveness		01	
	Time Management		02	
	Stress Management	5, 6	02	
	5.2 Start-up Skills Financial Literacy Risk Assessment Data Analysis (e.g. Consumer Behaviour, Market Trends, etc.)	2, 5	01	
6. Corporate Ethics	6.1 Intellectual Property Rights Copyrights Trademarks Patents	6	01	02
	6.2 Case Studies Cases related to Business/ Corporate Ethics	1 to 6	01	
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**28**

Activity No.	Activity/ Assignment Title (In the form of Short Notes, Questionnaire/ MCQ Test, Role Play, Case Study, Quiz, etc.)	Hrs/ Lab
1.	Test of English as Foreign Language (TOEFL)	02
2.	Group discussion (Practice session)-I	02
3.	Group discussion (Practice session)-II	02
4.	Final Group discussion-I	02
5.	Final Group discussion-II	02
6.	English Aptitude Test	02
7.	Resume Writing	02
8.	Mock interview	02
9.	Role play techniques for interpersonal skills	02
10.	Project Report Presentation-I	02
11.	Project Report Presentation -II	02
12.	Technical proposal	02
13.	Corporate Ethics/role play/case studies	02
14.	Business Meetings: case studies/role play	02
	Total:	**28**

Books:	
Text Books	1. Sanjay Kumar & PushpLata (2018). Communication Skills a workbook, New Delhi: Oxford University Press. 2. Bovée, C. L., & Thill, J. V. (2021). *Business communication today*. Upper Saddle River, NJ: Pearson.
Reference Books	1. Arms, V. M. (2005). Humanities for the engineering curriculum: With selected chapters from Olsen/Huckin: Technical writing and professional communication, second edition. Boston, MA: McGraw-Hill. 2. Butterfield, J. (2017). Verbal communication: Soft skills for a digital workplace. Boston, MA: Cengage Learning. 3. Masters, L. A., Wallace, H. R., & Harwood, L. (2011). Personal development for life and work. Mason: South-Western Cengage Learning. 4. Robbins, S. P., Judge, T. A., & Campbell, T. T. (2017). Organizational behaviour. Harlow, England: Pearson. 5. Meenakshi Raman, Sangeeta Sharma (2004) Technical Communication, Principles and Practice. Oxford University Press 6. Archana Ram (2018) Place Mentor, Tests of Aptitude for Placement Readiness. Oxford University Press
Useful Video links:	
1. TOEFL listening Skill https://www.youtube.com/watch?v=jSUh0Civuv4 2. MBA Interview https://www.youtube.com/watch?v=cwW9QBNuwCw 3. How to write a successful CV	

https://www.youtube.com/watch?v=U0JAfqEak2c

4. Interview techniques (How to answer tell me about yourself)
   https://www.youtube.com/watch?v=m5kR7TPAkSw
5. The 4 types of team members you can hire
   https://www.youtube.com/watch?v=5bYYFfpbSqc
6. Every Meeting Ever
   https://www.youtube.com/watch?v=K7agjXFFQJU

Assessment:

Term Work (25 Marks)

Term work of 25 Marks shall consist of a minimum 8 Assignments.

The distribution of marks for term work shall be as follows:

Assignment: 15 Marks

Book Report (hard copy): 10 Marks

Note: The final certification and acceptance of term work ensures the satisfactory performance of laboratory work and minimum passing in the term work.

Oral (25 Marks)

Oral Examination will be based on a GD & the Project/Book Report presentation.

1	Group Discussion: 10 Marks
2	Project Presentation: 15 Marks

Note:

1. The Main Body of the project/book report should contain a minimum **25 pages** (excluding Front and Back matter).
2. The group size for the final report presentation should not be less than 5 students or exceed 7 students.
3. There will be an end–semester presentation based on the book report.